IN THE CLAIMS:

1. A method for fabricating non-volatile memory cells, the method comprising:
forming a pillar of silicon vertically extending above a substrate;
implanting a drain region in a top of the pillar;
implanting first and second source regions in the substrate and adjacent to the pillar, wherein the first and second source regions are located on opposite sides of the pillar;
depositing a gate oxide on at least vertical sides of the pillar facing the first and second source regions;
forming floating gates adjacent to and on opposite sides of the pillar;
forming first and second control gates insulated from the floating gates and located on opposite sides of the pillar; and
forming a wordline parallel to and between the first and second control gates.

2. The method of claim 1 wherein the floating gates are fabricated using polysilicon.

3. The method of claim 1 wherein the control gates are fabricated using polysilicon and silicide.

4. The method of claim 1 wherein forming the pillar of silicon comprises etching the substrate to form first and second perpendicular grooves.

5. The method of claim 4 wherein the first groove is filled with an insulating material prior to etching the second groove.

6. The method of claim 5 wherein the source regions are generally located under the second grooves.

7. A method for fabricating a memory array, the method comprising:
etching a first series of parallel trenches in a substrate;
filling the first series of parallel trenches with oxide;
etching a second series of parallel trenches in the substrate, wherein the second series of parallel trenches are perpendicular to the first series of parallel trenches such that a plurality of substrate material pillars are formed and separated in a first direction by the oxide and a second direction by the second trenches;
implanting source regions at a bottom of the second parallel trenches;
implanting drain regions in the top of the pillars;
fabricating floating gates in the second trenches and insulated from the pillars;
fabricating control gates in the second trenches and insulated from the floating gates; and
fabricating a wordline parallel to and between the control gates.

8. The method of claim 7 wherein the floating gates and control gates comprise polysilicon.

9. The method of claim 7 wherein the control gates comprise a layer of polysilicon and a layer of tungsten.

10. The method of claim 7 further comprises:
fabricating vertically extending source contacts in electrical contact with the source regions;
fabricating conductive sources lines in electrical contact with the source contacts;
fabricating vertically extending drain contacts in electrical contact with the drain regions; and
fabricating conductive drain lines in electrical contact with the drain contacts.

11. A method for fabricating a memory array, the method comprising:
depositing a layer of nitride on a substrate;

etching a first series of parallel trenches in the layer of nitride;

filling the first series of parallel trenches with oxide by depositing a layer of thin oxide;

planarizing the layer of thin oxide with a chemical mechanical planarization process to remove the layer of thin oxide and leave the first series of parallel trenches filled with oxide;

etching a second series of parallel trenches in the substrate, wherein the second series of parallel trenches are perpendicular to the first series of parallel trenches such that a plurality of substrate material pillars are formed and separated in a first direction by the oxide and a second direction by the second trenches;

implanting source regions at a bottom of the second parallel trenches;

implanting drain regions in the top of the pillars;

fabricating floating gates in the second trenches and insulated from the pillars;

fabricating control gates in the second trenches and insulated from the floating gates; and

fabricating a wordline parallel to and between the control gates.

12. The method of claim 11 and further including depositing a layer of oxide on the substrate prior to depositing the layer of nitride.